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REMARKS

Claims 1-20 remain in the application.

Claims 1, 8, and 12 are amended to more particularly point out and distinctly claim the subject matter of the claims.

Claims 2, 4-7, 9-11, and 13 are amended to provide proper antecedent with the amendments to claims 1, 8, and 12.

Support for the amendments to the claims can be found at least on page 7, line 25 through page 8, line 2.

35 USC 102 Rejection:

Claims 1-8 and 10-20 were rejected under 35 U.S.C. 102 over U.S. patent publication no. US 2003/0197532 of inventor Tsuchida ("Tsuchida"). This rejection is respectfully traversed.

Amended claim 1 includes, among other things, configuring a first circuit of the self-gated transistor to disable the transistor substantially upon a positive current flow through the transistor and to enable the transistor responsively to a negative current flow through the transistor. At least this limitation is not disclosed by Tsuchida. Tsuchida is silent on a negative current flow through any of the transistors including transistors 4 and 5 (FIG. 6) and transistors 26 and 28 (FIG. 4). Also, Tsuchida does not disclose enabling any of the transistors, including transistor 26 (FIG. 4) and transistor 4 (FIG. 6), responsively to a negative current through a transistor. Yet claim 1 includes such a limitation. Thus, claim 1 should be allowable at least for these reasons. It is also believed that the reference voltages in FIG. 4 (reference 63) and FIG. 6 (positive input of comparator 9) have a

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polarity that prevents detecting such negative current flows. Additionally, Tsuchida does not disable either transistor 26 or transistor 4 substantially upon a positive current flow through the transistor. Tsuchida discloses that comparator 48 of FIG. 4 and comparator 9 of FIG. 6 are used to allow a positive current to flow through the transistor, if the positive current reaches a pre-determined threshold level they are then disabled. If the positive current does not reach the threshold level, the transistor remains enabled to conduct the positive current. Thus, Tsuchida does not disclose disabling the transistor substantially upon a positive current, but only disables the transistor upon the positive current reaching the threshold level. Please note Tsuchida paragraphs 0057 and 0040-0045. Accordingly, it is respectfully submitted that the relied on reference does not anticipate amended claim 1.

Claims 2-7 depend from claim 1 and are believed to be allowable for at least the same reasons as claim 1.

Additionally, claim 4 includes, among other features, coupling a comparator to receive the sense signal wherein the sense signal is positive for the positive current flow and is negative for the negative current flow. Tsuchida does not disclose a negative sense signal but only discloses a positive sense signal.

Further, claim 5 includes at least, coupling a non-inverting input of the comparator to have a negative offset voltage. The Office Action states in the second paragraph on page 3 that figure 6 shows the step of coupling a non-inverting input of the comparator to have a negative offset voltage. However, it should be noted that FIG. 6 shows a positive offset voltage applied to the non-inverting input of comparator 9. Thus, at least this limitation is not disclosed by Tsuchida.

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Claim 6 includes, coupling the comparator to responsively enable the self-gated transistor when the sense signal forms a voltage that is less than a voltage of a source of the self-gated transistor. Tsuchida does not disclose that the sense signal becomes less than the source of the self-gated transistor. It is believed that the sense signal of the circuits disclosed by Tsuchida can not form a sense signal at a potential that is less than a potential of the source of the self-gated transistor. For example, in FIG. 4 how can the sense signal become less than the value on the source of either transistor 26 or 28?

Amended claim 8 includes, among other things, configuring the self-gated transistor to conduct a second current through the sensing portion as a second sense signal wherein the second current flows in a direction opposite to the first current; and configuring the self-gate transistor to detect the second sense signal and responsively enable the self-gated transistor. At least these limitations are not disclosed by Tsuchida. The Office Action states in the last line of page 3 and continuing onto page 4 that "the direct (sic) of the current the (sic) flows through resistor 6 when transistor 5 is off". However, applicants respectfully submit that current does not flow through resistor 6 when transistor 5 is off. First, it should be noted that it is improper to modify the teaching of a reference from that which is taught by the reference. Additionally, applicants respectfully submit that the only current that flows through resistor 6 when transistor 5 is off can be leakage current from comparator 9 and that such current is in the positive direction through resistor 6 and that such direction is the same direction that positive current flows through resistor 6 when transistor 5 is enabled. If there is a portion of Tsuchida that discloses

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that current flows in an opposite direction through resistor 6 when transistor 5 is off, applicants respectfully request that such portion of the reference disclosing such be particularly pointed out or explained in an affidavit of the Examiner under MPEP 2144.03 and 37 CFR 1.111(d)(2). Thus, it is respectfully submitted that Tsuchida does not anticipate at least these limitations of amended claim 8.

Claims 10-11 depend from claim 8 and are believed to be allowable for at least the same reasons as claim 8.

Amended claim 12 has, among other features, a control circuit coupled to receive the sense signal and drive the first gate to enable the transistor responsively to a first polarity of the sense signal and to disable the transistor responsively to an opposite polarity of the sense signal. This limitation of claim 12 is not disclosed by the Tsuchida reference. Tsuchida enables and disables the transistor based on the value of a positive signal. Claim 12 calls for enabling and disabling the transistor base on the polarity (either negative or positive) of the current, not on the value of the positive current. This limitation is not disclosed by Tsuchida. Accordingly, it is respectfully submit that amended claim 8 is not anticipated by Tsuchida.

Claims 13-20 depend from claim 12 and are believed to be allowable for at least the same reasons as claim 12.

Also, claim 15 includes, the comparator has a negative offset. The deficiency of Tsuchida relating to this element was explained in the traversal of the 35 USC 102 rejection of claim 5 which is incorporated into this traversal of the rejection of claim 15 by reference.

Additionally, claim 20 includes, formed in a package having no greater than four leads. The Office Action states in the fourth paragraph of page 5 that a package having no greater than four leads is disclosed by FIG. 6. However, it

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should be noted that FIG. 6 is not complete, thus, the number of leads is indeterminate. At the minimum, the circuit of FIG. 6 requires a power input lead and probably requires a lead to enable switches 4 and 5. Consequently, the number of leads is not disclosed by the reference and it is merely speculation that the circuit of FIG. 6 is in a package having no more than four leads. Accordingly, it is respectfully submit that Tsuchida can not anticipate amended claim 8.

35 USC 103 Rejection:

Claim 9 was rejected under 35 U.S.C. 103 over Tsuchida in view of U.S. patent no. 5,422,593 issued to Fujihira ("Fujihira"). This rejection is respectfully traversed.

Claim 9 depends from claim 8 and includes all the limitations of claim 8. The deficiency of Tsuchida as applied to claim 8 is explained in the traversal of the 35 USC 102 rejection of claim 8. Combining Tsuchida with Fujihira does not make up for these deficiencies of Tsuchida. Thus, claim 9 should be allowable for at least the same reasons as claim 8.

The references cited but not relied upon were reviewed and are believed to not anticipate or make obvious applicants' claims.

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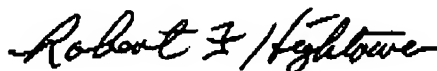
CONCLUSION

Applicant(s) made an earnest attempt to place this case in condition for allowance. In view of all of the above, it is believed that the claims are allowable, and that the case is now in condition for allowance, which action is earnestly solicited.

Although it is believed that no fees are due for this amendment, the Commissioner is hereby authorized to charge any fees that may be required or credit any overpayment to Deposit Account 50-1086.

If there are matters which can be discussed by telephone to further the prosecution of this Application, the Examiner is invited to call the undersigned attorney at the Examiner's convenience.

Respectfully submitted,
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